ABSTRACT

DETERMINING TIMING OF INTEGRATED CIRCUITS

A method of determining the timing of signal paths in a synchronous integrated circuit, taking into account the perturbing effect of switching in adjacent signal paths, the method comprising:

1) Forming predictions for timing delays in signal paths in the integrated circuit;

2) Selecting a first such path, tracing wires in the integrated circuit forming the path (victim wires) and determining adjacent and crossing wires thereto (aggressor wires);

3) For each aggressor wire, determining the amount of perturbation coupling to the victim wires of the first path;

4) Dividing the aggressor wires into a plurality of categories depending on the clocked timing of the aggressor wires in relation to the clocked timing of the victim wires;

5) Adding margins of error to the clocked timing of the victim wires in dependence upon the number of aggressor wires in one or more said categories.

Fig. 4